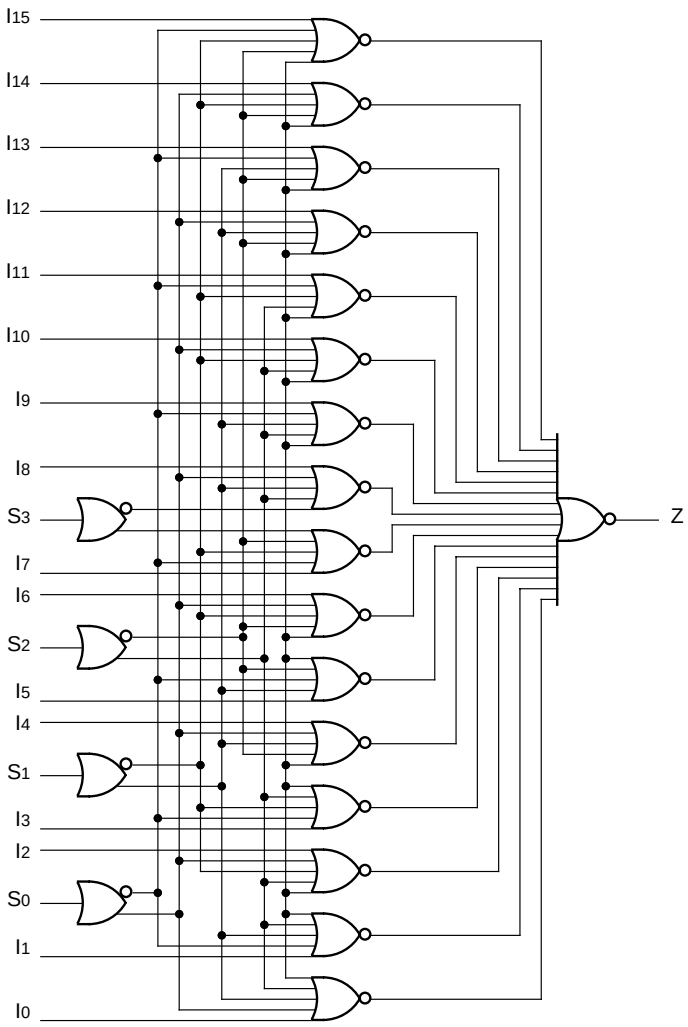
FEATURES

- **Max. propagation delay of 1300ps**
- **I_{EE} min. of –63mA**
- **Industry standard 100K ECL levels**
- **Extended supply voltage option: V_{EE} = –4.2V to –5.5V**
- **Voltage and temperature compensation for improved noise immunity**
- **Internal 75KΩ input pull-down resistors**
- **70% faster than Fairchild**
- **40% lower power than Fairchild**
- **Function and pinout compatible with Fairchild F100K**
- **Available in 24-pin CERPACK and 28-pin PLCC packages**

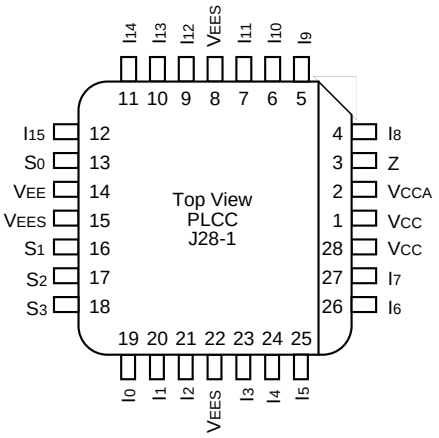
DESCRIPTION

The SY100S364 is a 16-input multiplexer designed for use in high-performance ECL systems. The four Data Select inputs (S_0, S_1, S_2, S_3) determine the bit from the 16 inputs (I_n) that will be passed on to the output as shown in the Truth Table. The output data polarity is the same as the input. The inputs on the device have 75KΩ pull-down resistors.

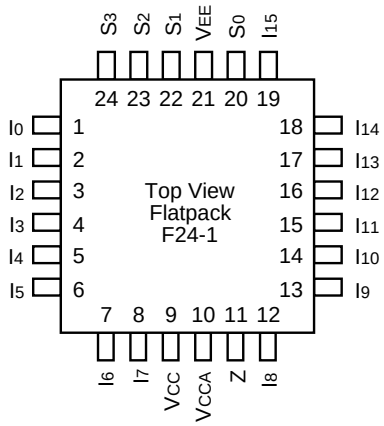
BLOCK DIAGRAM



PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)



24-Pin Cerpack (F24-1)

Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S364FC	F24-1	Commercial	SY100S364FC	Sn-Pb
SY100S364FCTR[1]	F24-1	Commercial	SY100S364FC	Sn-Pb
SY100S364JC	J28-1	Commercial	SY100S364JC	Sn-Pb
SY100S364JCTR[1]	J28-1	Commercial	SY100S364JC	Sn-Pb
SY100S364JZ[2]	J28-1	Commercial	SY100S364JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S364JZTR[1, 2]	J28-1	Commercial	SY100S364JZ with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Tape and Reel.
2. Pb-Free package is recommended for new designs.

PIN NAMES

Pin	Function
$I_0 – I_{15}$	Data Inputs
$S_0 – S_3$	Select Inputs
Z	Data Output
V_{EES}	V_{EE} Substrate
V_{CCA}	V_{CCO} for ECL Outputs

TRUTH TABLE(1)

Select Inputs				Output
S_0	S_1	S_2	S_3	Z
L	L	L	L	I_0
H	L	L	L	I_1
L	H	L	L	I_2
H	H	L	L	I_3
L	L	H	L	I_4
H	L	H	L	I_5
L	H	H	L	I_6
H	H	H	L	I_7
L	L	L	H	I_8
H	L	L	H	I_9
L	H	L	H	I_{10}
H	H	L	H	I_{11}
L	L	H	H	I_{12}
H	L	H	H	I_{13}
L	H	H	H	I_{14}
H	H	H	H	I_{15}

NOTE:

1. H = HIGH Voltage Level
   L = LOW Voltage Level

DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.5V unless otherwise specified; $V_{CC} = V_{CCA}$ = GND

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current				µA	$V_{IN} = V_{IH}$ (Max.)
	I_n	—	—	200		
	S_0, S_1	—	—	200		
	S_2, S_3	—	—	200		
I_{EE}	Power Supply Current	–63	–45	–30	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERPACK

V_{EE} = –4.2V to –5.5V unless otherwise specified; $V_{CC} = V_{CCA}$ = GND

Symbol	Parameter	$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay $I_0 – I_{15}$ to Output	400	1400	400	1400	400	1400	ps	
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to Output	400	1900	400	1900	400	1900	ps	
t_{PLH} t_{PHL}	Propagation Delay S_2, S_3 to Output	400	1700	400	1700	400	1700	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

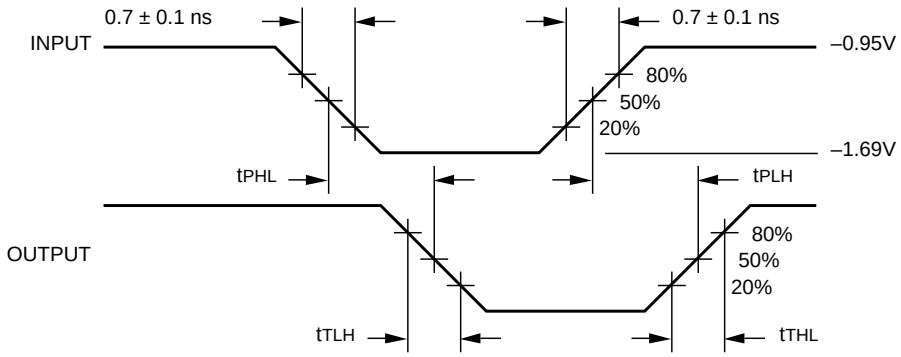
AC ELECTRICAL CHARACTERISTICS

PLCC

V_{EE} = –4.2V to –5.5V unless otherwise specified; V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay I_0 – I_{15} to Output	400	1300	400	1300	400	1300	ps	
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to Output	400	1800	400	1800	400	1800	ps	
t_{PLH} t_{PHL}	Propagation Delay S_2, S_3 to Output	400	1600	400	1600	400	1600	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

TIMING DIAGRAM

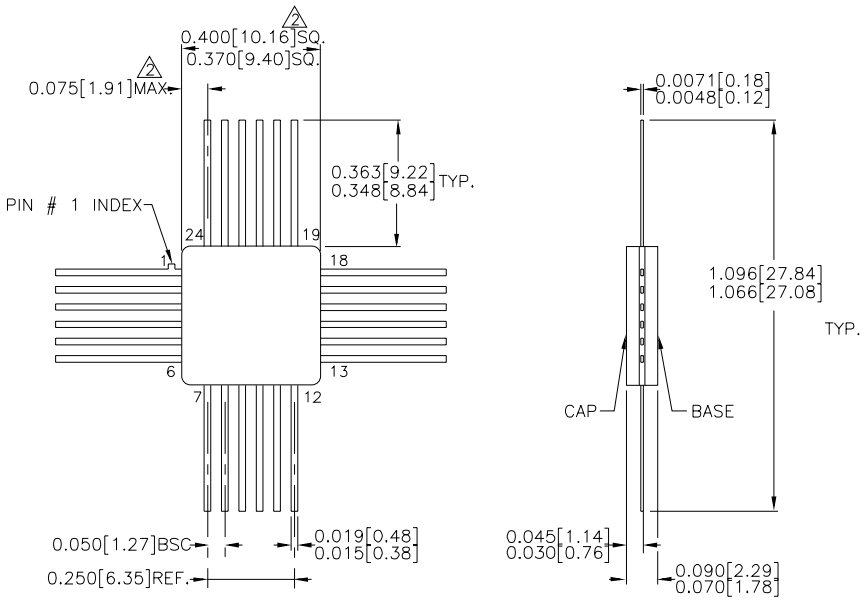


Propagation Delay and Transition Times

Note:

V_{EE} = –4.2V to –5.5V unless otherwise specified; V_{CC} = V_{CCA} = GND

24-PIN CERPACK (F24-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

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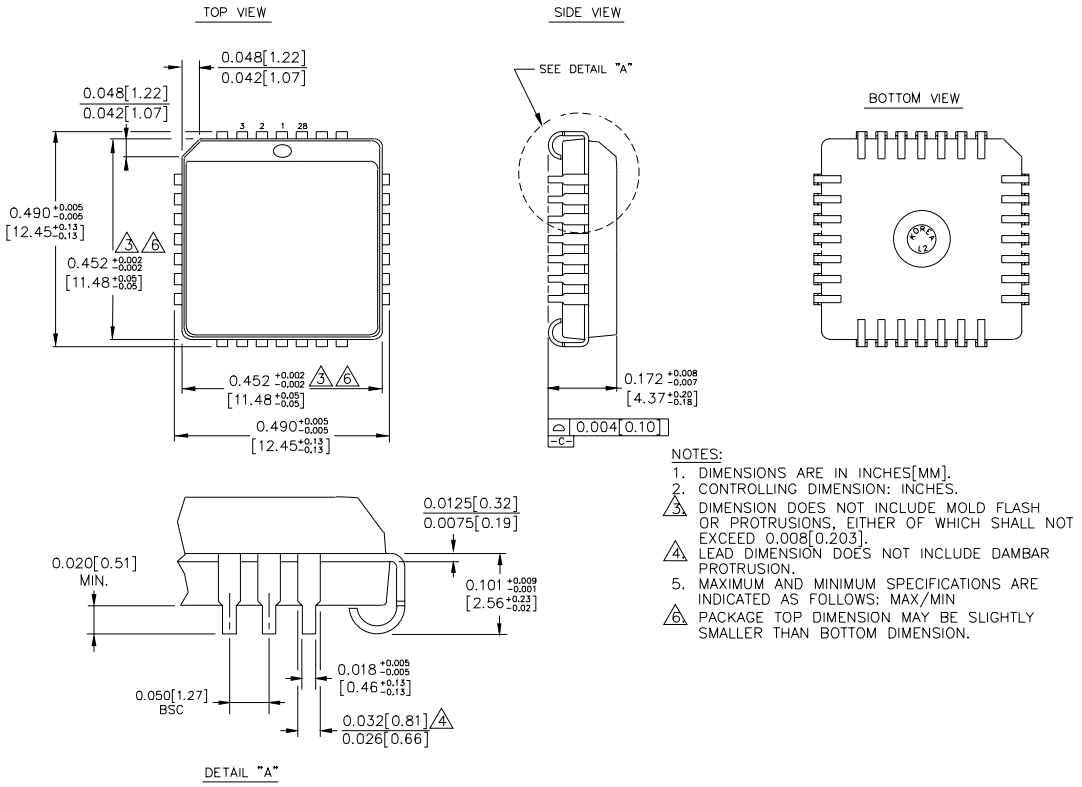
28-PIN PLCC (J28-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. 03

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